WHAT IS CLAIMED IS

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1. A circuit, comprising:

a register which stores therein a semaphore address; and

a semaphore control circuit which asserts a control signal in response to a read access by a processor directed to the semaphore address, and negates the control signal in response to a write access by the processor directed to the semaphore address.

2. The circuit as claimed in claim 1, further comprising a comparator which makes a comparison of an address output from the processor with the semaphore address stored in said register, and asserts a match signal when the comparison indicates a match, wherein said semaphore control circuit includes:

a circuit which sets the control signal to an asserted state in response to assertion of the match signal and an indication of a read operation by a read/write signal output from the processor; and

a circuit which resets the control signal to a negated state in response to the assertion of the match signal and an indication of a write operation by the read/write signal output from the processor.

3. The circuit as claimed in claim 1, wherein a right to use a bus given to the processor is not relinquished in response to a bus-arbitration request supplied from an external source during an asserted state of the control signal.

4. The circuit as claimed in claim 3, further comprising a bus-arbitration control circuit which receives a signal indicative of the bus-arbitration request, the control signal, and a chip enable signal output from the processor, said bus-arbitration control circuit operating not to assert a bus-arbitration-acknowledge signal in response to the bus-arbitration request signal regardless of a state of the chip enable signal if the control signal is in an asserted state, operating not to assert the bus-arbitration-acknowledge signal in response to the bus-arbitration request signal if the chip enable signal is in an asserted state and the control signal is in a negated state, and operating to assert the bus-arbitration-acknowledge signal in response to the bus-arbitration request signal if the chip enable signal is in a negated state and the control signal is in the negated state.

5. A processor, comprising:
a processor core;
a register which stores therein a semaphore address; and
a control circuit which asserts a control signal in response to a read access by said

processor core directed to the semaphore address, and negates the control signal in response to a write access by said processor core directed to the semaphore address.

6. The processor as claimed in claim 5, wherein said control circuit includes:

a comparator which makes a comparison of an address output from said processor core with the semaphore address stored in said register, and asserts a match signal when the comparison indicates a match;

a circuit which sets the control signal to an asserted state in response to assertion of the match signal and an indication of a read operation by a read/write signal output from said processor core; and

a circuit which resets the control signal to a negated state in response to the assertion of the match signal and an indication of a write operation by the read/write signal output from said processor core.

7. The processor as claimed in claim 5, wherein a right to use a bus is not relinquished in response to a bus-arbitration request supplied from an external source during an asserted state of the control signal.

8. A multi-processor system, comprising:

a plurality of processors;

a memory shared by said plurality of processors; and

a semaphore register for controlling exclusive use of said memory, wherein at least one of said plurality of processors includes:

a processor core;

an address register which stores therein an address of said semaphore register; and

a control circuit which asserts a control signal in response to a read access by said processor core directed to the address stored in said address register, and negates the control signal in response to a write access by said processor core directed to the address stored in said address resister.

9. The multi-processor system as claimed in claim 8, wherein said control circuit includes:

a comparator which makes a comparison of an address output from said processor core with the semaphore address stored in said address register, and asserts a match signal when the comparison indicates a match;

a circuit which sets the control signal to an asserted state in response to assertion of the match signal and an indication of a read operation by a read/write signal output from said processor core; and

a circuit which resets the control signal to a negated state in response to the assertion of the match signal and an indication of a write

operation by the read/write signal output from said processor core.

10. The multi-processor system as claimed in claim 8, wherein said at least one of said plurality of processors does not relinquish a right to use a bus in response to a bus-arbitration request made by another one of the processors during an asserted state of the control signal.